// VerilogA for ADC\_FinalProject, B\_SubADCLogic, veriloga

`include "constants.vams"

`include "disciplines.vams"

module B\_SubADCLogic(C2,C1,ph2,S1,S2,S3,B2,B1,vdd,vss);

parameter real clk\_th=0.9;

parameter real delay = 0;

parameter real ttime = 1p;

inout vdd,vss;

input C2,C1,ph2;

output S1,S2,S3,B2,B1;

electrical vdd,vss;

electrical C2,C1,ph2;

electrical S1,S2,S3,B2,B1;

real ss1,ss2,ss3,bb2,bb1;

analog begin

@(cross(V(ph2) - clk\_th, +1)) begin

if ((V(C2)>0.9) && (V(C1)>0.9)) begin

ss1 = V(vdd); ss2 = V(vss); ss3 = V(vss);

bb2 = V(vdd); bb1 = V(vss);

end

else if ((V(C2)<0.9) && (V(C1)>0.9)) begin

ss1 = V(vss); ss2 = V(vdd); ss3 = V(vss);

bb2 = V(vss); bb1 = V(vdd);

end

else begin

ss1 = V(vss); ss2 = V(vss); ss3 = V(vdd);

bb2 = V(vss); bb1 = V(vss);

end

end

@(cross(V(ph2) - clk\_th, -1)) begin

ss1 = V(vss); ss2 = V(vss); ss3 = V(vss);

end

V(S1) <+ transition(ss1,delay,ttime);

V(S2) <+ transition(ss2,delay,ttime);

V(S3) <+ transition(ss3,delay,ttime);

V(B2) <+ transition(bb2,delay,ttime);

V(B1) <+ transition(bb1,delay,ttime);

end

endmodule